Final

JOINT STATEMENT OF THE 22nd MEETING OF THE WORLD SEMICONDUCTOR COUNCIL (WSC)

MAY 24th, 2018
San Diego, California, USA

The world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, Korea, and the United States – held the 22nd meeting of the World Semiconductor Council (WSC) today in San Diego, California.

The meeting was chaired by Mr. Matt Murphy of Marvell Semiconductor, Inc. and chair of the host delegation, the Semiconductor Industry Association in the United States. The other delegations attending the 22nd WSC meeting – Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, and Korea – were chaired, respectively, by Mr. Zhao Haijun of Semiconductor Manufacturing International Corporation, Mr. Ching-Jiang Hsieh of MediaTek, Mr. Jens Knut Fabrowsky of Robert Bosch GmbH, Mr. Testuya Tsurumaru of Renesas, and Mr. Seung Kook Synn of SKhynix.

The WSC meets annually to bring together industry leaders to address issues of global concern to the semiconductor industry. The WSC's mandate is to encourage cooperation to promote fair competition, open trade, protection of intellectual property, technological advancement, investment liberalization, market development, and sound environmental, health and safety practices. The WSC also supports expanding the global market for information technology products and services.

Established under the "Agreement Establishing a New World Semiconductor Council" signed on June 10, 1999, and amended on May 19, 2005, the WSC has the goal of promoting cooperative global semiconductor industry activities in order to facilitate the healthy growth of the industry from a long-term global perspective. This Agreement states, "the increasing globalisation of the semiconductor industry raises important issues that must be addressed effectively through

international cooperation within the world semiconductor industry", and that "the WSC activities . . . shall be guided by principle of fairness, respect for market principles, and consistency with WTO rules and with the laws of the respective countries or regions of each Member. The WSC recognizes that it is important to ensure that markets will be open without discrimination. The competitiveness of companies and their products should be the principal determinant of industrial success and international trade."

The WSC seeks policies and regulatory frameworks that fuel innovation, propel business, and drive international competition and avoid any actions that distort markets and disrupt trade. Antitrust counsel was present throughout the meeting. During the meeting, the below reports were given and discussed, and related actions were approved.

I. Cooperative Approaches in Protecting the Global Environment

The WSC is firmly committed to sound and positive environmental policies and practices. The members of the WSC are proactively working together to make further progress in this area.

(1) PFC (Perfluorocompound) Emissions

The global semiconductor industry is a very minor contributor to overall emissions of greenhouse gases, and the industry is continuously working to further reduce our contribution to emissions of GHGs. One important part of our GHG emission reduction efforts is our voluntary reduction of PFC gas emissions. In 1999, the WSC (consisting at that time of each of the original regional semiconductor associations in the U.S., the European Union, Japan, Korea, and Chinese Taipei) agreed to reduce PFC emissions by at least 10% below individual baselines for each regional semiconductor association by the end of 2010. The WSC has previously announced that, the industry had far surpassed this goal. Over the 10-year period, the WSC has achieved a 32% reduction. In 2011, the WSC (consisting of the five regional semiconductor associations in the 1999 agreement, with the addition of SIA in China) also announced a new voluntary PFC agreement for the next 10 years. The elements of the 2020 goal include the following:

- The implementation of best practices for new semiconductor fabs. The industry expects that the implementation of best practices will result in a Normalized Emission Rate (NER) in 2020 of 0.22 KgCO2e/cm^2 equivalent to a 30% NER reduction from 2010 aggregated baseline. Best practices will be continuously reviewed and updated by the WSC.

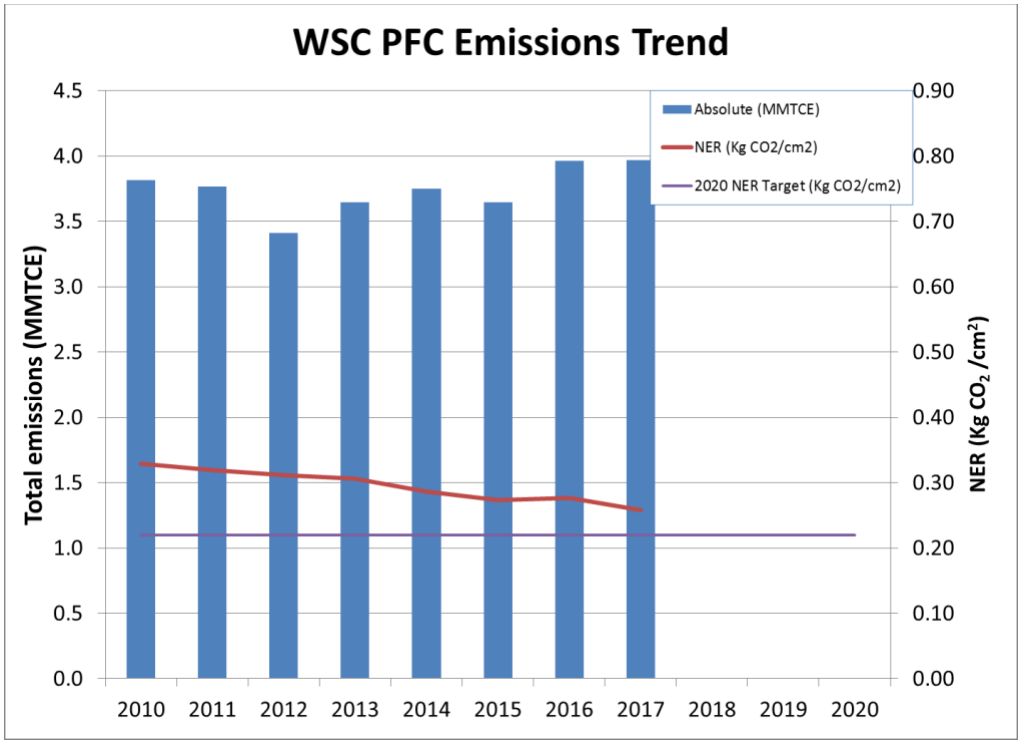
- The addition of "Rest of World" fabs (fabs located outside the WSC regions that are operated by a company from a WSC association) in reporting of emissions and the implementation of best practices for new fabs.

- A NER based measurement in kilograms of carbon equivalents per area of silicon wafers processed (KgCO2e/cm^2) that will be a single WSC goal at the global level.

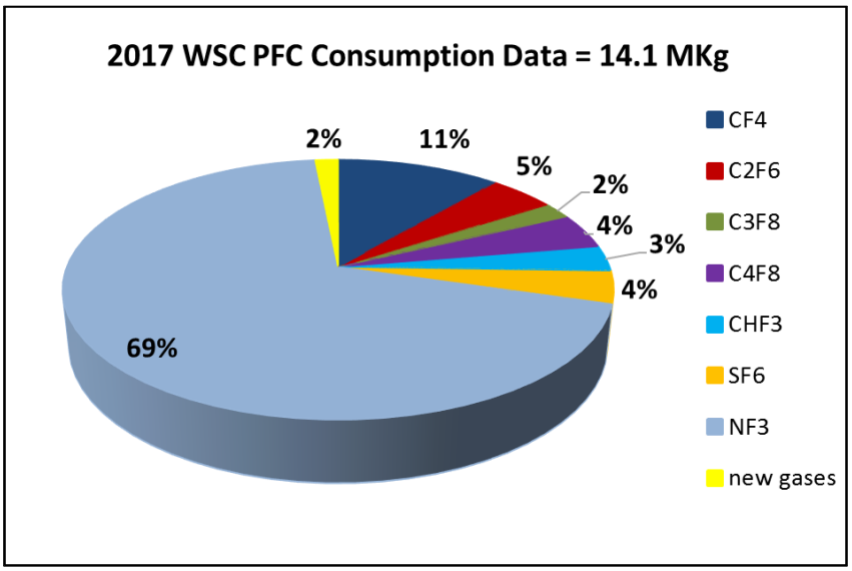
The WSC agreed to report its progress on this new voluntary agreement on an annual basis. This external reporting will provide aggregated results of the absolute PFC consumption and emissions alongside each other and NER trends. These figures represent combined emissions for the six WSC regional associations, in their own regions and in the "Rest of World" fabs described above. In addition, to improve transparency, the WSC has made its Best Practices for PFC Reduction document available previously on the WSC website. In 2016 the WSC has also revised its best practices document and published this update on the WSC website. The 2017 reporting also includes the reporting of newly used gases CH_2F_2, C_4F_6, C_5F_8 and C_4F_8O. In addition, the WSC reports the individual gas breakdowns.

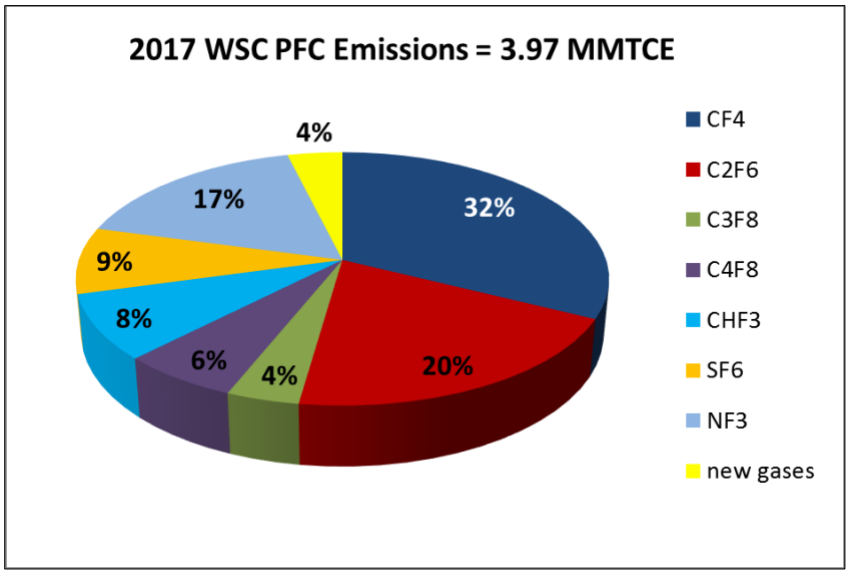
The seventh-year results are as follows: in 2017, combined WSC absolute emissions of PFCs increased by 3.9% above 2010 to 3.97 MMTCE in 2017. The NER decreased by 21.6 % compared to 2010 and decreased 7% below 2016. Please see the graph below which compares these results to 0.22Kg/cm^2 equivalent to a 30% NER reduction anticipated by 2020.

Results of WSC PFC Emission Trends



2017 WSC PFC Consumption and Emissions Data





The WSC is encouraged by the overall trends in reducing normalized PFC emissions in the semiconductor industry. We note, however, that achieving these reductions is becoming increasingly challenging due to a number of factors. These factors include: increased process complexity, which sometimes requires the use of additional and different gases; the addition of new gases (e.g., CH_2F_2, C_4F_6, C_5F_8 and C_4F_8O), which represent about 4% of WSC emissions; and different measurement and reporting methods, such as the updated reporting regulations in the U.S.

In order to ensure the continued accuracy of WSC reporting on PFC emissions, the WSC notes that it will continue working with the Intergovernmental Panel on Climate Change (IPCC) on the process to update the guidelines applicable to reporting of emissions from semiconductor fabs and to reflect the most current and best available data.

(2) Chemical Management

The WSC acknowledges the environmental and health concerns associated with perfluorooctanoic acid (PFOA) and related substances. In response to the concerns raised by the global environmental and health community, the WSC commits to work to transition away from the use of PFOA and PFOA related substances in semiconductor manufacturing.

The global semiconductor industry has a demonstrated record of achievement in phasing-out the use of chemicals of concern, such as the industry's successful efforts to phase out perfluorooctanyl sulfonates (PFOS).[1] As a follow-up to our successful efforts on PFOS, the WSC is committing to transitioning away from the use of PFOA and PFOA related substances in chemical formulations in semiconductor manufacturing. The process of identifying and qualifying replacement chemicals can be extremely complex and it is essential that companies be given sufficient time to work through this process. The WSC intends to complete this work by a target date of 2025. However, additional time may be needed to complete the final replacement process for PFOA related substances due the complexity of replacing these substances in all applications.

The WSC is aware that governments around the world are considering taking action on other chemicals of interest to the semiconductor industry. Despite our industry's success in phasing out PFOS, **the WSC reiterates its recommendation that Governments/Authorities proceed carefully in regulating chemicals that are essential to the semiconductor industry.**

The WSC recommends that Governments/Authorities take into account the limited potential risk of exposure from uses in the semiconductor industry and our supply chain, the management practices in the semiconductor industry, the small quantity of chemicals used in manufacturing processes or contained in articles, and the fact that these chemicals are not intended to be released from the finished product under normal conditions of use. The WSC recommends that any regulations provide the semiconductor industry with sufficient time to evaluate our uses of chemicals that may be subject to potential regulation and the uses within our supply chain. If restrictions on chemicals used in our industry are deemed to be necessary and appropriate for the protection of human health and the environment, the WSC recommends that Governments/Authorities provide sufficient time for the industry to identify, qualify, and transition to alternative chemicals that satisfy our functional and performance requirements, and be provided with exemptions to allow continuation of critical uses of these chemicals in processes and articles. In addition, where regulations cover articles,

[1] In 2011, the WSC announced that it successfully eliminated non-critical uses of PFOS in its manufacturing operations and identified substitutes for most other uses. In 2017, the WSC announced that the companies participating in the WSC successfully eliminated the remaining uses of PFOS in semiconductor manufacturing.

the threshold levels in regulations should be harmonized globally and be technically feasible.

As part of our industry's proactive approach to promote worker health and safety in the semiconductor industry and protect the environment, the WSC requests that individual companies and their suppliers work collaboratively and on a voluntary basis to increase the disclosure of chemicals present in products supplied to the industry. Specifically, the WSC calls on suppliers to take voluntary action to disclose information about the presence of regulated substances in their products even if these substances are below regulatory thresholds that would mandate disclosure. The disclosure of information, consistent with existing and evolving regulatory requirements, will help enable the industry to develop the most effective programs to protect worker health and safety and the environment and to act more effectively on new information. More information on this topic is found in Annex 1.

(3) Resource Conservation

Semiconductor devices contribute to improved resource conservation in our world. Energy efficiency enabling semiconductors play a key role in the more efficient transmission, distribution and consumption of energy which also largely contributes to world's carbon emission reduction, contributing to humankind's achieving the United Nation's carbon reduction goal under the global climate change risk mitigation.

Traditional forms of energy and renewable energy sources will not be sufficient alone to meet the world's future energy needs. Consuming energy more efficiently is therefore of paramount importance, and semiconductor devices help achieve this goal. Semiconductor devices enable a more efficient use of energy in all aspects of our daily lives: in the home, office or on the road; in industrial manufacturing; in public infrastructure; and in public transport. The semiconductor sector itself is not a large natural resource consumer amongst global industries. However, the WSC's members continue to focus activity on reducing the use of resources involved in the device manufacturing processes to reduce the direct impacts to the local and global environment. The semiconductor sector will continue to pursue environmental conservation programs in its fabs in the areas of energy, water and waste and the industry will continue to share examples of improvement practices.

In order to help the global semiconductor industry to continue to improve its environmental performance, the WSC calls on suppliers of equipment to the semiconductor industry, including wet-clean tool suppliers, to design equipment that is more efficient and generates less waste. Individual semiconductor companies and their equipment suppliers have worked closely with each other on a voluntary basis to improve the efficiency and environmental performance of our industry's manufacturing processes, and this collaboration must continue so that efficiency improvements keep pace with increased process complexity and the resulting increase in resource consumption, consistent with global and governmental regulations, policies and/or goals. We request the equipment suppliers to the semiconductor industry work to design their equipment, including wet-clean tools, to work more efficiently in the use of resources and generate less waste.

In some instances, governments/authorities are requesting the submission of proprietary data as part of environmental reporting programs. In order to provide governments/authorities with necessary information while also preventing the disclosure of this sensitive information, **the WSC recommends that governments/authorities ensure that environmental reporting programs are structured in a manner that allows the indirect reporting of manufacturing information in certain circumstances, and prevents disclosure of confidential business information (CBI)**. More information on this recommendation is found in Annex 2.

II. Semiconductor Market Data

The WSC reviewed the semiconductor market report covering global market size, market growth, and other key industry trends. According to WSTS data, in 2017, the global semiconductor market totaled $412.2B in revenue and grew year-over-year by 21.6 percent. Several products stood out in 2017. Memory was the largest semiconductor category by sales with $124.0 billion and the fastest growing with sales increasing by 61.5 percent. Logic ($102.2 billion) and micro-ICs ($63.9 billion) -- a category that includes microprocessors -- rounded out the top three product categories in terms of total sales. Other fast-growing product categories in 2017 included rectifiers (18.3 percent), diodes (16.4 percent), and sensors and actuators (16.2 percent). Annual sales increased substantially across all regions:

the Americas (35.0 percent), China (22.2 percent), Europe (17.1 percent), Asia Pacific/All Other (16.4 percent), and Japan (13.3 percent). From an end use perspective, Communication (32.0 percent) and Computer (30.3 percent) remained the largest end markets by share, followed by Consumer (13.6 percent), Industrial (12.1 percent), and Automotive (11.0 percent).

III. Customs and Tariffs

A. Implementation of the Information Technology Agreement (ITA) and ITA expansion

The WSC applauded the conclusion of the ITA expansion agreement in 2015, which mandated tariff-free treatment for a wide range of semiconductor products, including advanced devices such as Multi-component Integrated Circuits (MCO) and Multi-chip Integrated Circuits (MCP).

The WSC is grateful to GAMS for addressing, in its 2017 meeting, ITA implementation and the challenge created by new import tariffs imposed by some customs authorities on certain MCOs in conjunction with the update to the 2017 World Customs Organization (WCO) Harmonised System. The WSC supports the GAMS conclusion that duties should not increase, irrespective of changes to the HS, as this is not in line with ITA commitments. **The WSC strongly encourages GAMS to ensure that any existing tariffs on products - such as MCOs - that were duty-free under the ITA are eliminated immediately and to ensure that implementation happens in a transparent and WTO conforming way.**

B. Review of the ITA scope

The WSC strongly supports continuously updating the ITA product scope to include new and evolving semiconductor technologies, as this would minimize administrative burden and ensure a barrier-free movement of goods across borders, both of which are crucial for the semiconductor industry. Despite the recent ITA expansion, there are still semiconductor products excluded from the current ITA and ITA expansion coverage.

The WSC welcomes the invitation by GAMS to provide updates on advances in semiconductor technology with a view to maintaining duty-free treatment on semiconductors as technology evolves. The WSC is working on suggestions for

future updates to the ITA scope. When Government/Authorities decide to update the ITA, the WSC will support the corresponding negotiations.

To maximize the benefits of the ITA and ITA expansion, the WSC also calls on GAMS to encourage additional WTO members to join those Agreements. Broader membership in ITA and ITA expansion will more quickly intensify the benefits of the ITA for all members. Finally, WSC calls on GAMS to encourage all ITA and ITA expansion parties to consider autonomously eliminating tariffs on semiconductor products earlier than foreseen in the staging schedule.

C. Semiconductor-based transducers and MCP

The WSC reiterates its appreciation for GAMS' endorsement of the definition for semiconductor-based transducers proposed for an amendment to HS 8541 by the WSC in 2016. For the purposes of this definition, semiconductor-based transducers are semiconductor-based sensors, semiconductor-based actuators, semiconductor-based resonators and semiconductor-based oscillators.

The WSC welcomes the progress made in the World Customs Organisation (WCO) on the semiconductor-based transducers definition. **The WSC urges GAMS to continue to support the semiconductor-based transducer proposal and cooperate with its Customs agencies to agree on the corresponding amendment to heading 8541 so that it can be implemented within the HS2022 review.**

The WSC is working with Customs agencies and the WCO to include a modified definition of MCP products (clarifying that also products in which not all ICs are electrically interconnected will be considered as MCP) and appreciates that customs authorities in the EU support this work by bringing this topic into the WCO. The WSC requests GAMS to continue to work with their WCO delegates in order to gain support for the proposal submitted by the EU, for approval and implementation within the HS 2022 review cycle.

D. Customs Classification for Semiconductors

The WSC remains committed to working with GAMS customs agencies and the World Customs Organisation to achieve uniform customs classification of all semiconductor products under the HS headings dedicated to semiconductors.

The WSC would like to reiterate that the gap between rapid innovation in semiconductor technology and the multi-year HS nomenclature international alignment processes has resulted in HS definitions that are complex and difficult to administer or do not cover new innovative products. As a consequence, differing interpretations can occur, which can result in classification inconsistencies or in semiconductor products being classified outside of the semiconductor HS headings 8541 and 8542, in spite of the direction in Note 9 of Chapter 85 which states "For the classification of the articles defined in this note, headings 8541 and 8542 shall take precedence over any other heading in the Nomenclature." This can lead to more administrative burden both for Authorities and industry, and can risk giving rise to disputes.

The WSC illustrated in detail the above issues in letters to the WCO in 2015 and 2016, during the GAMS meetings and during a meeting with customs agencies from the GAMS regions on 16 March 2017. Based on these exchanges and meetings, the WSC has started analysing potential challenges . The WSC endeavours to provide GAMS updates on the outcome of the WSC work in this area.

E. Trusted Traders

Semiconductor companies continue to invest substantially to comply with trusted traders' policies worldwide, such as the Authorised Economic Operators' (AEO) programs. These policies aim to enhance compliance and supply chain security coupled with bolstering smooth, fast and efficient import and export processes. Most semiconductor companies have achieved AEO status, many of them in multiple jurisdictions worldwide.

The WSC welcomes the GAMS' support for enhanced cooperation with customs authorities to strengthen the AEO programmes and enhance tangible trade facilitation for trusted traders. The WSC appreciates the GAMS acknowledgment of the importance of global alignment of compliance and supply chain security programmes, and their further mutual recognition.

In response to the GAMS request, the WSC is currently working on articulating best practices on AEO/Trusted Traders programs and endeavours to share them with GAMS ahead of the GAMS 2018 meeting.

The WSC is also engaged in exchanges with Customs authorities from GAMS regions regarding the organisation of a separate meeting in 2019 on the sidelines of an international Customs meeting. The WSC encourages GAMS to work with their Customs authorities to ensure that all GAMS regions participate in such meeting.

III. Regional Support Programs

The WSC welcomes GAMS' support for full implementation of the *Regional Support Guidelines and Best Practices*, which reflect the shared view that the competitiveness of companies and their products, and not the intervention of governments and authorities, should be the principal driver of industry success and international trade.

The WSC has noted a significant increase in government assistance to the semiconductor industry in recent years, and shares concerns with GAMS that market-distorting subsidies and other types of non-market-based support by governments and government-related entities will have a significant disruptive impact on the development of the semiconductor industry. Such practices can lead to excess capacity that is not commercially justified, create unfair competitive conditions, hinder innovation, and undermine the efficiency of global value chains.

Recognizing the important role of transparency for developing market-based responses by industry and governments to changing market conditions, the GAMS and WSC developed the *Regional Support Guidelines and Best Practices* to promote the active sharing of data on subsidies and other government support. Such transparency is vital to sustainable growth of the global semiconductor industry, and for the effective adherence to the principles of fairness, respect for market principles, and consistency with WTO rules as enshrined in the WSC Charter**.**

Consistent with the 2017 GAMS Chair Summary, the WSC has undertaken a self-assessment starting with five programs or measures per jurisdiction. A significant amount of information has been shared between all WSC regions, indicating a recognition by the WSC regarding the importance of transparency. Where gaps remain, WSC regions commit to continuing to gather information on

the identified programs, and will share with GAMS prior to the announced GAMS intercessional.

Due to notable gaps in information regarding government programs that have a significant impact on the global semiconductor market, per the 2017 GAMS Chair Summary, the WSC requests that GAMS members be prepared to provide further transparency and details on identified programs, where industry was unable to provide such detail. Furthermore, we request the GAMS discuss and evaluate these programs or measures with respect to consistency with WTO rules, the *Regional Support Guidelines and Best Practices,* and any negative effects or potential negative effects on the semiconductor industry at the 3rd Workshop on Regional Support at the 2018 GAMS Meeting. The WSC requests that GAMS members identify appropriate officials or individuals responsible for or familiar with government support programs in their region to participate in this workshop. The WSC looks forward to a productive discussion and information exchange, and presents to GAMS its proposed workshop agenda, attached in Annex 3.

WSC further welcomes the GAMS commitment to continue discussions of related issues with a bearing on government support, such as investment, anti-monopoly rules, or IP issues, during regular inter-sessional work and at the 2018 workshop.

As a step toward full implementation of the *Regional Support Guidelines*, the WSC also requests that GAMS members promptly notify GAMS and the WTO of all programs identified in the WSC self-assessment that are subject to the full WTO notification requirements as contemplated by Article 25 of the WTO/(SCM) Agreement, and ensure that information on the programs or measures is complete and publicly available online.

IV. Encryption Certification & Licensing Regulations

The WSC welcomes the GAMS' support for the WSC Encryption Principles, which emphasize market access, transparency, adoption of international standards, and non-discriminatory and open procedures and rules for commercial encryption. The WSC further commends the GAMS for encouraging

all governments to take the WSC Encryption Principles into account to avoid a negative impact on the industry's competitiveness and prevent unnecessary restrictions to trade. The WSC emphasizes that the WSC Encryption principles should apply to all commercial applications including most critical information infrastructure (CII) applications. Allowing the use of commercial cryptography in connected products used in CII enables cost-effective support for business continuity.

In line with the GAMS Chair's Summary, the WSC underscores the need for all governments/authorities to make use of international standards and to use open procedures when setting standards for commercial encryption, allowing international stakeholders to collaboratively participate in the definition of such standards. Open markets and the application of International standards ensure the worldwide availability of the most robust and trusted security solutions and support the diffusion of emerging encryption technologies. Participation of international stakeholders in the formulation of standards for commercial encryption remains the best method to achieve rigorously scrutinized encryption technology and thus also facilitate trade in line with the WSC principles.

The WSC welcomes the call by GAMS to review the global regulatory environment for commercial encryption. As requested by GAMS the WSC has undertaken a self-assessment and started evaluating the relevant regional existing and planned laws, regulations and other measures in relation with the WSC Encryption Principles. The results allow to identify a significant number of laws, administrative measures, and other rules, both draft and in force, which shape the regulatory and policy frameworks on commercial encryption worldwide.

The WSC encourages GAMS to continue to discuss how the WSC Encryption principles can be best applied to commercial encryption, including CII. Furthermore, the WSC requests GAMS to discuss and assess the existing and planned laws, regulations and other measures on commercial encryption with respect to conformity to the WSC Encryption principles and in particular whether any of the laws or regulations or other measures constitutes an unnecessary barrier to trade. Such discussions should take place during the intersessional work and 2018 GAMS meeting.

The WSC is grateful to the Japanese Chair for the initiative to organise a GAMS workshop on encryption at the GAMS in October 2018, and requests each GAMS member to ensure appropriate expert participation in the workshop. Further, the WSC presents to GAMS its proposed workshop agenda, attached in Annex 4.

V. Effective Protection of Intellectual Property

A. Patent Quality

The quality of patents is crucial to the continued growth and innovation of the semiconductor industry. The WSC recognizes the importance of improving patent quality and has been working with WIPO and the patent offices of GAMS members to encourage the collection and dissemination of standardized statistical metrics bearing on patent examination quality. The WSC has adopted ten (10) recommendations to GAMS for improving patent examination quality, along with suggested benchmarks for measuring performance on each recommended practice.

The WSC recommended Best Practices on patent quality address the following topics: (1) Examination Quality Review; (2) Appropriate Workload; (3) Adequate Funding; (4) Resources and Support; (5) Training and Qualification Requirements; (6) Faster Administrative Procedures; (7) Post-Grant Review Mechanism; (8) Cooperation Between Patent Offices; (9) Examination Procedures; and (10) Transparency and Cooperation with WIPO on Patent Examination Metrics. These WSC recommendations on Patent Quality are attached as Annex 5.

The WSC urges governments and authorities to distribute these best practices recommendations to all relevant government entities within each jurisdiction. The WSC calls on governments and authorities to support these Best Practices in the operation of their respective patent offices and to improve the quality of patents that are issued.

B. Abusive Patent Litigation (NPEs/PAEs)

The WSC recognizes that abusive patent litigation seriously undermines innovation by redirecting research expenditures and other resources to unnecessary litigation expenses, and by making it more difficult to bring products to market. The WSC supports the continued focus on preventing abusive patent litigation.

In view of this, the WSC encourages a range of "best practices" in regard to the issue of abusive patent litigation, including NPEs/PAEs. As a result, the WSC adopted a set of *"Abusive Patent Litigation (Including NPEs/PAEs): Best Practices to Combat Abusive Patent Litigation"* as set forth in Annex 2 to the WSC's 2017 Joint Statement.

The WSC calls on governments and authorities to support these Best Practices in addressing abusive patent litigation practices.

C. Trade Secrets

The WSC supports national legislative initiatives to improve the protection of trade secrets. The WSC reminds government and authorities to support and implement "Core Elements for Trade Secret Protection Legislation" in Annex 1 to the 2015 WSC Joint Statement, when making the national trade secret protection legislation, and any related pending legislation or legislative reforms or amendments. The WSC will continue discussions on this topic.

VI. Fighting the Proliferation of Semiconductor Counterfeiting

The proliferation of counterfeit semiconductor products creates serious risks to the safety and health of the public and to critical national infrastructure and can have a significant economic impact for semiconductor rights holders.

The WSC remains committed to intensify anti-counterfeiting work activities through its Anti-Counterfeiting Task Force. This Task Force has produced the WSC's White Paper "Winning the Battle against Counterfeit Semiconductor Products" that describes the risks from counterfeit products. The WSC's White Paper is currently

being updated with new sections outlining the counterfeit threat that is facilitated by the online environment and examples of counterfeit products. The collision of the online economy and globalization has created a perfect environment for counterfeiters, allowing them to sell counterfeit goods directly worldwide with virtually no barriers to entry, low cost of set up and fewer risks of being caught. The WSC supports pro-active online enforcement activities to remove trade mark infringing and counterfeit semiconductors from online platforms. The WSC will continue to increase the awareness of the public safety and infrastructure risks caused by semiconductor counterfeits when dealing with authorities and at international conferences. The WSC Anti-Counterfeiting Task Force has also shared anti-counterfeiting capacity building measures that could be employed across the semiconductor industry. The WSC Anti-Counterfeiting Task Force will continue its efforts in these areas.

The WSC supports the Global Anti-Counterfeiting Group's (GACG) World Anti-Counterfeiting Day on June 6, 2018 which aims to increase the awareness of the safety and health risks caused by counterfeits. Please refer to Annex 6.

The WSC appreciates the GAMS' statement at its 2017 meeting, underlining the GAMS' commitment to fighting semiconductor counterfeiting and to work with their customs and law enforcement authorities to intensify the implementation of semiconductor anti-counterfeiting enforcement measures. The WSC looks forward to continued coordination with GAMS in stopping counterfeits and will continue to cooperate with GAMS customs and enforcement authorities in these efforts.

The WSC calls on GAMS members to continue to implement appropriate measures (including domestic, bilateral and multilateral countermeasures) to deal with counterfeit semiconductors. The WSC supports GAMS members in employing proactive enforcement measures, including strict search and seizure, and working closely with the industry and also welcomes GAMS coordination with their customs and law enforcement authorities.

VI. Conflict Minerals

The WSC adopted at its 17th meeting in May 2013 a Conflict-Free Supply Chain Policy in order to support the global progress in addressing the sourcing of conflict minerals from conflict zones, such as the Democratic Republic of the Congo

(DRC) and surrounding countries[2]. The global semiconductor industry is a recognized leader in addressing conflict minerals. The semiconductor industry has been involved in the development of compliance tools (such as the OECD due diligence guidance framework) that have been readily adopted by other key industry sectors and has implemented state of the art programs to track progress.

In 2018 to reflect the current status of the conflict minerals topic and its broad geographical scope, the WSC has agreed to update its policy statement of 2013. This update of the conflict-free supply chain policy references the deep concerns about the sources of minerals from 'conflict-affected and high risk areas' which goes beyond the original focus of the policy statement on the 'Democratic Republic of the Congo (DRC) and surrounding countries' and again underlines that the global semiconductor industry is committed to using 'responsibly sourced' minerals in their semiconductor products. This update emphasizes the importance of supply chains acting responsibly to source minerals and agrees that the WSC will promote the 'OECD Due Diligence Guidance for Responsible Supply Chains of Minerals from Conflict-Affected and High-Risk Areas' among its members to do this. The OECD guidance serves as a common reference for all stakeholders in the mineral supply chain in order to clarify expectations concerning the nature of responsible supply chain management of minerals from conflict-affected and high-risk areas. The 2018 updated WSC policy statement now reads:

> *There are increased societal concerns with the mining of certain minerals used in the semiconductor industry. The WSC shares the deep concern about sources of minerals from these conflict-affected and high-risk areas.*
>
> *WSC members are committed to use responsibly sourced minerals in their products. To meet this objective, the WSC underlines the importance of a comprehensive due-diligence process aligned with other initiatives within the global industry to achieve a responsible supply chain. The WSC will promote the use of the OECD Due Diligence Guidance for Responsible Supply Chains of Minerals from Conflict-Affected and High-Risk Areas[3], common tools, methods and standards among WSC member associations on this issue.*

The WSC also welcomes the certification of more global smelters and refiners through the Responsible Minerals Initiative Assurance Process as a positive

[2] "surrounding countries" as defined under the Dodd-Frank Wall Street Reform Act 2012 (Central Africa Republic, South Sudan, Zambia, Angola, The Republic of the Congo, Tanzania, Burundi, Rwanda, Uganda)

[3]Conflict-Affected and High-Risk Areas' as outlined in the OECD (2016), OECD Due Diligence Guidance for Responsible Supply Chains of Minerals from Conflict-Affected and High-Risk Areas: Third Edition.

development. The WSC would recommend that if GAMS members are considering new conflict minerals type legislation, that the legislation should be globally aligned to ensure that such legislations promote the harmonization of global efforts for creating responsible supply chain management of minerals from conflict-affected and high-risk areas and should utilize existing industry-wide compliance tools (such as the OECD due diligence guidance framework) and initiatives (such as (Responsible Minerals Initiative) and be based on voluntary principles.

VII. Growth Initiative

The WSC is committed to initiatives aimed at accelerating the rate that semiconductor technologies are adopted in emerging sectors, including sharing published research, engaging in dialogue with other industry sectors and regulators, issuing reports on emerging application markets, and advocating for public policies and agreements that promote growth.

As part of this initiative, the WSC organized an experts panel session on Artificial Intelligence (AI), focusing on new applications and implications for the semiconductor industry. The WSC presented a special report on AI focusing on adoption growth, economic trends, R&D investments, and policy implications. The AI semiconductor market is projected to top $30 billion in the next 5 years. Three invited panelists presented their views on the implications and impact of AI on the semiconductor industry in terms of technology development, policy, and opportunities for industry growth.The speakers included 1) Dr. Jeff Welser, Vice President & Lab Director, IBM Research- Almaden 2) Dr. Kai Yu, Founder & CEO, Horizon Robotics, and 3) Dr. Rajesh Pankaj, Senior Vice President of Engineering, Qualcomm.

As highlighted in the presentations, semiconductors are a driving force in the AI revolution that will have an enormous global economic impact over the next 20 years. The WSC supports innovative technologies and public policies that will advance AI and other emerging sectors that have potential for economic and societal benefits.

In addition to the policy recommendations included elsewhere in this Joint Statement, the WSC encourages governments and authorities to help enable new and innovative semiconductor technology applications by:

1. **Supporting basic and pre-competitive R&D to overcome technical challenges, especially in the areas of low-power computing, energy efficient sensing, security of connected systems, storage, and wireless connectivity.**
2. **Promoting interoperability by adopting technology-neutral policies, and working together to create common standards/policies for wireless connectivity, storage, data security, encryption, etc.**
3. **Working with industries so that regulations in fields such as automotive and health care encourage investment in and adoption of new digital processes/technologies.**
4. **Supporting policies that open markets and streamline trans-border data flow, including eliminating tariffs on next-generation semiconductors and ICT products.**
5. **Supporting a positive WTO agenda on e-commerce and digital trade to obtain specific progress on issues of vital interest to our industry and respective economies. Such opportunities include increasing ITA participation and product coverage, and promoting environmental goods.**

VIII. Approval of Joint Statement and Approval of Recommendations to GAMS

The results of today's meeting will be submitted by representatives of WSC members to their respective governments/authorities for consideration at the annual meeting of WSC representatives with the Governments/Authorities Meeting on Semiconductors (GAMS) to be held in October 2018 in Chiba, Japan.

IX. Next Meeting

The next meeting of the WSC will be hosted by the Semiconductor Industry Association in China and will take place in Xiamen City on May 23, 2019.

X. Key Documents and WSC Website:

All key documents related to the WSC can be found on the WSC website, located at: http://www.semiconductorcouncil.org

Information on WSC member associations can be found on the following websites:

Semiconductor Industry Association in China:
http://www.csia.net.cn

Semiconductor Industry Association in Chinese Taipei:
http://www.tsia.org.tw

Semiconductor Industry Association in Europe:
http://www.eusemiconductors.eu

Semiconductor Industry Association in Japan:
http://semicon.jeita.or.jp/en/

Semiconductor Industry Association in Korea:
http://www.ksia.or.kr

Semiconductor Industry Association in the US:
http://www.semiconductors.org

Annexes:

1. **Chemical Disclosure by Suppliers**
2. **Confidential Information and Environmental Reporting**
3. **Proposed Agenda for 3rd GAMS Workshop on Regional Support**
4. **Proposed Agenda for GAMS Workshope on Encryption**
5. **WSC Press Release: WSC supports World Anti-Counterfeiting Day**
6. **WSC Recommendations to Patent Offices for Improving Patent Quality**

Annex 1

Chemical Disclosure by Suppliers

As part of our industry's proactive approach to promote worker health and safety in the semiconductor industry and protect the environment, the WSC requests that individual semiconductor companies and their suppliers work on a voluntary basis to increase the disclosure of chemicals present in products supplied to the industry. Specifically, the WSC calls on suppliers to take voluntary action to disclose information about the presence of regulated substances in their products even if these substances are below regulatory thresholds that would mandate disclosure. The disclosure of information, consistent with existing and evolving regulatory requirements, will help enable the industry to develop the most effective programs to protect worker health and safety and the environment and to act more effectively on new information.

Suppliers provide their customers, such as semiconductor manufacturers, with information on the chemical composition of their products in documents known as safety data sheets (SDSs). Legal requirements may vary around the world, but laws typically set forth threshold levels that mandate reporting of a chemical substance in a chemical formulation. If a particular chemical substance is below the reporting threshold, the chemical may not be disclosed in the SDS. As a result, a chemical that is relevant for purposes of assessing worker exposure may be present in a chemical mixture sold to the semiconductor industry, but the specific chemical might not be disclosed in the SDS.

To improve our industry's protection of human health and the environment, the WSC encouages individual semiconductor manufacturers to work with their chemical suppliers on a voluntary basis to support disclosure of information on all chemicals in a product, even if the chemical is present in concentrations below applicable regulatory thresholds. Such disclosure should inform manufacturers on information such as the presence of impurities, derivatives, and other relevant information about chemicals of concern, and consistent with existing and evolving regulatory requirements, will help enable the industry to develop the most effective programs to protect worker health and safety and the environment and to act more effectively on new information . Such disclosure should be included in the SDS if possible, but if this information is a trade secret, it should be disclosed in a separate document that can be protected from public disclosure. The WSC

requests that suppliers enter into company-to-company agreements to protect any information that may be deemed a trade secret.

Working together, the global semiconductor industry and its suppliers can help protect workers from exposure to chemicals of concern.

Annex 2

Confidential Information and Environmental Reporting

The WSC recommends that governments/authorities ensure that environmental reporting programs are structured in a manner that allows the indirect reporting of manufacturing information in certain circumstances, and prevents disclosure of confidential business information (CBI).

Data on mask layers is highly confidential business information in the semiconductor industry. This information is confidential because a company could gain insights into manufacturing methods of a competitor. Accordingly, this information is carefully guarded from disclosure and should not be required to be reported as part of an environmental reporting program. Detailed information about input values, including number of mask layers, needed to document compliance could be provided upon audit or inspection, under conditions of confidentiality.

The WSC recommends governments/authorities avoid requiring the reporting of competitive information such as the number of mask layers as part of environmental reporting regulations. Such data may be properly included in a reporting program as an input into a broader normalization calculation, such as including number of mask layers as one input into a calculation that also includes production output, but without the number of mask layers being reported independently. For example, in normalizing wastewater discharges, a legitimate approach would be to divide the amount of discharge by the product of output (in square centimeters (cm^2)) by the number of mask layers, without either of these values being reported independently. This approach would enable normalized performance values to be submitted to governments/authorities without risking the disclosure of valuable company CBI.

The WSC believes that such a reporting approach would not compromise the environmental goals of emission control and environmental quality management of governments/authorities.

Annex 3

3rd Government and Authorities Meeting on Semiconductors (GAMS) Workshop on Regional Support Programs

October 16, 2018

AGENDA

Time	Meeting	Speaker
9:00-9:10	**Welcome and Introduction by GAMS Chair**	**Japan GAMS Chair**
9:10-9:30	**WSC Presentation/Remarks** • GAMS Regional Support Guidelines & Best Practices • WSC Self-Notification/Information Exchange	**2018 WSC Chair (SIA in US)**
9:30-12:30	**WSC Self-Assessment Discussion (Japan, China, Chinese Taipei)** • Reports/Presentations on Regional Support Programs by Program Managers or Government/Industry Experts • Q&A • Discussion	Moderator: Speakers: GAMS, program managers, industry experts
12:30-13:30	**Lunch**	
13:30-16:30	**WSC Self-Assessment Discussion (EU, Korea, US)** • Reports/Presentations on Regional Support Programs by Program Managers or Government/Industry Experts • Q&A • Discussion	Moderator: Speakers: GAMS, program managers, industry experts
16:30-16:45	**Break**	
16:45-17:30	**Summary & Conclusions** • Discussion	Moderators
17:30	**Closing Remarks, Adjourn**	**Japan GAMS Chair**

Annex 4

GAMS Workshop on Encryption

Wednesday, October 17, 2018
at Sheraton Grande Tokyo Bay

Attendees: delegates and experts from the GAMS and the WSC

Proposed Draft Agenda

16:00 – 16:10	**Opening remarks**	GAMS Chair (Japan)
16:10 – 16:30	**WSC report on WSC activities on encryption**	WSC Chair (SIA in the US)
16:30 – 17:45	• **Individual presentations by each WSC region on the results of the *WSC Self-Assessment Survey on Encryption*** • **Q & A session: questions by GAMS and their experts**	All WSC member associations (5/7 minutes each) GAMS delegates and their experts, WSC delegates
17:45 – 18:15	• **Understanding encryption regulations: Exchange of views among GAMS on encryption in the GAMS regions**	GAMS delegates and their experts
18:15 – 18:30	**Closing remarks**	GAMS Chair (Japan)

Remark: 18:30 - 19:30 GAMS Welcome Reception

Annex 5

WSC Recommendations to Patent Offices for Improving Patent Quality

The quality of patents is crucial to the continued growth and innovation of the semiconductor industry. The WSC recognizes the importance of improving patent quality and has been working with WIPO and the patent offices of GAMS members to encourage the collection and dissemination of standardized statistical metrics bearing on patent examination quality. Set forth below are ten recommendations from the WSC for improving patent examination quality, along with some suggested benchmarks for measuring performance on each recommended practice:

1. Examination Quality Review

Background: Even when armed with adequate technology, legal knowledge and support, there is no guarantee that an examiner's performance will be up to standard.
Recommendation: The WSC recommends that POs set up proper performance review program, with an objective measurement scale, to periodically evaluate examiners' examination quality. Poorly-performing examiners should be given support and closer supervision, and where poor performance continues should be transitioned away from examination duties.
Applicable Metrics: Actual average examination time per application (from filing until issuance as patent or abandonment) in the prior year, Average case load per examiner (Patent apps/examiner) in the prior year, Examiner turnover ratio in the prior year, Overturned internal appeals v. total internal appeals.

2. Appropriate Workload

Background: Even the best, most efficient examiners need enough time to review and examine applications, conduct prior art searches, communicate with applicants and to do the necessary administrative work. Certain technologies may take examiners longer to review.
Recommendation: The WSC recommends that POs should determine the average time for properly examining a patent application and recruit enough examiners based on the number of annual patent applications filed within the previous year or as forecasted.
Applicable Metrics: Actual average examination time per application (from filing until issuance as patent or abandonment) in the prior year, Average number of hours allocated to examine an application.

3. Adequate Funding

Background: All factors bearing on patent quality are dependent on adequate funding. Without adequate funding, it may not be possible for POs to hire an appropriate number of examiners, to adequately train them, and arm them with the necessary resources and technology to perform at a high level. Adequate funding is therefore crucial. Yet funding needs should not impose an undue burden on applicants by way of fees such that they become an obstacle to innovation. On the other hand, fees collected from the applicants by the POs should not be used for other purposes than supporting the work of the POs

Recommendation: The WSC recommends that Governments should provide sufficient funding to POs to maintain adequate headcount, up-to-date hardware, software and technology, and adequate training and periodic evaluation. The WSC stands ready to lend its support to any PO in advocating for adequate budgets from its responsible authority.

Applicable Metrics: All metrics referenced in these Recommendations relevant to adequate funding.

4. Resources and Support

Background: Probably most important among patent quality factors is the accuracy of the patent scope (patent claims). In order to determine what the "newly invented" technology is, examiners need to find the most relevant existing technologies (the prior arts) for purposes of comparison. The internet provides access to worldwide documents, but convenience sometimes also causes trouble - too many references for the examiners to choose from. In addition, when a new application relates to cutting-edge or highly specialized technology, examiners may have difficulty properly evaluating the value of the new invention.

Recommendation: The WSC recommends that POs should provide examiners with access to all important technology databases, in addition to patent databases. Examiners should keep a record of searched database for each case and statistics should be collected and made publicly available. POs should also consider ensuring up-to-date technology, such as the best search engine, is available for examiners to use. POs should implement an internal support system so that examiners can easily seek internal help. If appropriate, POs should also consider outsourcing all or part of the prior-art search work to reliable third party search firms. POs should use best practices in using outside experts for technology support in examination and post-grant review processes.

Applicable Metrics: Average number of database searched per case

5. Training and Qualification Requirements

Background: Examination of patent applications requires examiners to evaluate technical documents under legal standards. Technology evolves over time, as do legal standards. Examiners should be equipped with up-to-date technology and legal knowledge.
Recommendation: The WSC recommends that POs should regularly review and modify their training programs, and qualification processes for new examiners. POs should set up objective evaluation processes and standards to qualify new examiners, and only those who pass the evaluation should be allowed to examine patent applications. POs should also design and implement continuing education courses for all active examiners. Poorly-performing examiners should be given support and closer supervision, and where poor performance continues should be transitioned away from examination duties.
Applicable Metrics: Number of apps pending, Full time/part time examiner ratio in the prior year, Examiner turnover ratio in the prior year, Number of technical training hours per year/examiner.

6. Faster Administrative Procedures

Background: Although in average examiners spend only a few days to examine one patent application, it takes years for applicants to receive a formal disposition (grant, rejection). The administrative procedures, the backlog of older applications, and the time for applicants to respond to office actions all contribute to long delays in the examination process.
Recommendation: The WSC recommends that patent offices (POs) periodically review their internal procedures and determine which steps can be simplified and/or streamlined. POs should implement a paperless environment and should encourage applicants to use an electronic filing process, whenever feasible. It is also recommended that POs should develop a strategy to clear the backlog of pending applications periodically.
Applicable Metrics: Number of apps pending at year end, Average time of first office action (from filing to first office action or search report) in the prior year, Average period of time (in months) from filing until final disposition in prior year, Actual average examination time per application (from filing until issuance as patent or abandonment), Average case load per examiner (Patent apps/examiner) in total, and average cases added annually to case load in the prior year, Average number of hours allocated to examine an application

7. Post-Grant Review Mechanism

Background: It is, of course, unrealistic to expect all patent examinations to be perfect given limited time and resources. Some patent claims will be erroneously allowed. In recognition of this, most POs have implemented a post-grant review mechanism to invalidate erroneously granted claims, but most of these mechanisms limit the evidence that challengers can adduce in the review process. For example, in some countries challengers may only present printed publications to POs during post-grant review. It is also not unheard of that some companies use post-grant review to block competitors' patents without providing threshold evidentiary support.
Recommendation: The WSC recommends that POs develop and implement robust post grant review procedures, including steps to verify the legitimacy of evidence so that challengers may present various types of evidence. POs also should conduct a threshold review of challenge requests and determine whether there is sufficient evidence to warrant initiation of a post-grant review.
Applicable Metrics: Number of patents invalidated in the prior year versus patents granted.

8. Cooperation between POs

Background: The Patent Prosecution Highway (PPH) speeds up the examination process for corresponding applications filed in cooperating POs. Through PPH, an applicant who receives a positive ruling on patent claims from one participating PO can request accelerated prosecution of corresponding claims in another participating PO. This allows applicants to obtain a patentability decision in the second office more quickly. The examiner in the office of later examination (OLE) can reuse the search and examination results from the office of earlier examination (OEE), thereby reducing workload and avoiding duplication of effort. Nonetheless, the search and examination results of a rejected application can also be very useful for the examiner in OLEs to properly examine counterpart applications.
Recommendation: The WSC recommends that POs should actively participate in PPH programs. POs should also cooperate by sharing search and examination results of all patent applications (including rejected applications), which may require mandatory disclosure of foreign counterpart applications by the applicants.
Applicable Metrics: Number of patents issued through PPH/year

9. Examination Procedures

Background: a patent application (claim) needs to meet certain legal standards – eligible subject matter, novelty, non-obviousness (inventive step) – in order to be patentable. When there are no detailed and objective guidelines on how to apply

these legal standards, examiners may tend to make judgments based on their subjective viewpoint. Applicants also need to know the applicable guidelines in order to communicate efficiently with the examiners.
Recommendation: The WSC recommends that POs publish detailed, objective guidelines on how to properly determine the patentability of claims. These guidelines should provide step-by-step instructions into the examination procedures for each legal standard, and should be updated periodically to reflect current law.
Applicable Metrics: Public availability of patentability guidelines (y/n?), and published periodic updating (y/n?).

10. Transparency and Cooperation with WIPO on Patent Examination Metrics

Background: The WSC has been collaborating with WIPO and the patent offices of GAMS members to identify standardized statistical metrics bearing on patent quality and to encourage the annual collection and dissemination of such statistical information. The WSC has published a list of 12 patent quality metrics, and WIPO has recently amended its annual IP statistical questionnaire to add a module for collecting patent examination statistics. These metrics cover workload, examination outcome, patent examiners, pendency time and post-examination opposition procedures. [See Attachment for relevant pages from the WIPO questionnaire.]
Recommendation: Mindful that the circumstances of each PO are unique, the WSC nonetheless believes that maintaining and reporting a broad array of pertinent examination-related statistics, and the comparative publication of these statistics, can serve as a useful benchmark for assessing and improving global patent examination.
The WSC urges each PO to ensure transparency of statistics related to its annual examination of patents. The WSC also urges POs to cooperate with WIPO in responding to its annual patent quality statistical questionnaire, and in periodically reviewing, augmenting and improving the statistical metrics bearing on patent examination quality. Finally the WSC commends WIPO for coordinating this statistical initiative and encourages it to continually strive to enhance its collection of patent quality statistics.

Annex 6

6 June 2018

FOR IMMEDIATE RELEASE

WSC supports World Anti-Counterfeiting Day

On 6 June 2018, the Global Anti-Counterfeiting Group (GACG) Network is celebrating the 20th edition of the World Anti-Counterfeiting Day (WACD). The World Semiconductor Council (WSC) strongly supports the WACD and believes it is a great initiative to highlight the anti-counterfeit measures being taken across industries. The World Anti-Counterfeiting Day enables the organisation of various events focusing on particular problems of counterfeiting & piracy under the umbrella of an international outreach campaign. This year's Global Anti-Counterfeiting Awards ceremony will also be held in Paris, France on WACD, 6 June 2018.

In 2012, the WSC has established an Anti-Counterfeiting Task Force amongst the semiconductor industry associations of China, Chinese Taipei, Europe, Japan, Korea, and the United States, with the aim of promoting activities to fight counterfeiting, incl. training, awareness raising, and encouraging purchases from authorised sources. The WSC works closely with governments and authorities on policies and regulations, and encourages domestic, bilateral and multilateral counter-measures and enforcement activities. Such enhanced anti-counterfeiting cooperation activities at the industry level alongside government agencies, customs and law enforcement agencies is instrumental to identify and stop parties involved in manufacturing or trafficking in counterfeit goods. A recent EU Joint

Customs Operation on counterfeit semiconductors highlighted the ongoing illicit challenges the industry continues to face in this area[4].

According to the Organisation for Economic Co-operation and Development (OECD), international trade in counterfeit goods represented up to 2.5% of world trade, or up to USD 461 billion[5]. In view of these staggering numbers, the WSC is convinced by the importance of an initiative such as the World Anti-Counterfeiting Day, and believes it to be a great way of highlighting the common cause of fighting counterfeiting – industry sectors alongside well-informed customers, and national enforcement authorities.

About WSC

The World Semiconductor Council is a cooperative body of the world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, Korea and the United States – that meets annually to address issues of global concern to the semiconductor industry. The WSC also meets annually with the governments and authorities of the six regions to convey industry recommendations. The WSC is dedicated to the principle that markets should be open and competitive and works to encourage policies and regulations that fuel innovation, propel business and drive international competition in order to maintain a thriving global semiconductor industry.

More information on the WSC is available at http://www.semiconductorcouncil.org

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[4] EU Anti-Fraud Office (OLAF), Press release 3/7/2017. https://ec.europa.eu/anti-fraud/media-corner/news/03-07-2017/olaf-helps-partners-seize-over-one-million-counterfeit-semiconductors_en

[5] Figures for 2013. Source: Organisation for Economic Co-operation and Development (OECD)–European Union Intellectual Property Office (EU IPO) (2016), *Trade in Counterfeit and Pirated Goods. Mapping the Economic Impact*, http://www.gacg.org/media/documents/201/041816_Mapping_the_Economic_Impact_en.pdf.